What is Claimed is:

1. An integrated circuit capacitor comprising:

a lower electrode on an integrated circuit substrate, the lower electrode comprising a metal layer on the integrated circuit substrate and hemispherical grain lumps that protrude from the metal layer opposite the integrated circuit substrate;

a dielectric layer on the hemispherical grain lumps opposite the integrated circuit substrate; and

an upper electrode on the dielectric layer opposite the lower electrode;

wherein the metal layer and the hemispherical grain lumps comprise at least one of Pt, Ru, Rh, Os, Ir and Pd.

2. The capacitor of Claim 1, wherein the dielectric layer comprises at least one of Ta_2O_5, $SrTiO_3$(STO), (Ba, Sr)TiO_3(BST), $PbTiO_3$, Pb(Zr, Ti)O_3(PZT), $SrBi_2Ta_2O_5$(SBT), (Pb, La)(Zr, Ti)O_3, $Bi_4Ti_3O_{12}$, or $BaTiO_3$(BTO).

3. The capacitor of Claim 1, wherein the metal layer comprises a first portion and a second portion on the first portion, and wherein the first and second portions comprise different metals.

4. The capacitor of Claim 3, wherein the first portion comprises at least one of TaN, Ti, and TiN.

5. The capacitor of Claim 4, wherein the second portion comprises at least one of Pt, Ru, Rh, Os, Ir and Pd.

6. The capacitor of Claim 4, wherein the first portion comprises a first material, and wherein the second portion comprises a second material that is more readily oxidized than the first material, under same oxidizing conditions.

7. The capacitor of Claim 3, wherein the first portion comprises Pt, and wherein the second portion comprises at least one of Ru, Rh, Os and Pd.

8. The capacitor of Claim 1, wherein the metal layer comprises a first portion and a second portion on the first portion, which both comprise a same metal,

and wherein the first portion retains it surface morphology when forming the hemispherical grain lumps.

9. The capacitor of Claim 8, wherein the metal layer comprises at least one of Pt, Ru, Rh, Os, Ir and Pd.

10. The capacitor of Claim 1, wherein the lower electrode further comprises a metal layer on the integrated circuit substrate between the hemispherical grain lumps or the substrate and the metal layer, and the metal layer is sufficiently thin so as to maintain the profile of the hemispherical grain lumps.

11. The capacitor of Claim 10, wherein the hemispherical grain lumps comprise at least one of Pt, Ru, Rh, Os, Ir and Pd.

12. The capacitor of Claim 10 wherein the hemispherical grain lumps comprise at least one of Ru, Rh, Os, Ir and Pd.

13. The capacitor of Claim 1, wherein the lower electrode comprises a metal layer on the substrate and a metal oxide layer on the metal layer opposite the substrate, and the hemispherical grain lumps protrude from the metal oxide layer opposite the metal layer.

14. The capacitor of Claim 13, wherein the metal layer comprises at least one of Pt, Ru, Rh, Os, Ir and Pd.

15. An integrated circuit capacitor comprising:

a lower electrode on an integrated circuit substrate, the lower electrode comprising a metal layer on the integrated circuit substrate and hemispherical grain lumps that comprises at least one noble metal and that protrude from the metal layer opposite the integrated circuit substrate;

a dielectric layer on the hemispherical grain lumps that comprise at least one noble metal, opposite the integrated circuit substrate; and

an upper electrode on the dielectric layer opposite the lower electrode.

16. The capacitor of Claim 15, wherein the metal layer comprises a first portion and a second portion on the first portion, and wherein the first and second portions comprise different metals.

17. The capacitor of Claim 16, wherein the first portion comprises at least one of TaN, Ti, and TiN.

18. The capacitor of Claim 17, wherein the second portion comprises at least one of Pt, Ru, Rh, Os, Ir and Pd.